

U 924 数字串行I0模块 用户手册

版本号: 1.0

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MegaSig

- 一、 硬件说明
- 1. U 924拥有1组输入和1组输出,接口类型: HD-15
 - a) 面板接口采用为HD-15;
 - b) 独立的主时钟、位时钟和帧时钟
 - c) 拥有4个Data;
 - d) 可选择信号的格式,字宽,位深



HD-15

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- 二、 软件界面操作说明
- 1. 1. 此说明为使用SIO Lab软件里DSIO模块具体说明使用,其他使用操作可参考SIO Lab手册

①打开SIO Lab软件,软件分为输出和输入两组配置。 选择连接方式: Digital Serial IO,以及对应U924设备 选择增加测试项目

🖳 SIO Lab - V2.0.2.61	-	0	×
file Language Report Remote Help			
MegaSig + _			
Signal Path: Signal Path 0 🐃 Add Test Delete Test			
Output Configuration Concector A28 Device U 922 U 923 Output Chandel Control Chi Q Enable Chi Q Enable Chi Q Enable Chi Q Enable Chi Q Conduct Statefors Journal State - 700 Simulus Device - 700 Simulus Device - 700 Simulus Device - 700 Output Sample Rate - 900 (ASS - 17) - VAN Verification - 900 (ASS - 17)			
Input Configuration ^ Concector	put: A28	(16 Ch)2	24kHz

②点击选Advanced Setting,此处配置Digital Serial IO模块的参数设置

🐺 SIO Lab - V2.0.4.27														- 0
File Software Setting Language	Tool About													
megasig														
Signal Path: Signal Path 0 🛛 🗸	&Meters 1 Add Test Delete Test													
Output Configuration ^	<													
Connector	Output Value	Monitor Ch0	Ch1 Total											
Digital Serial IO 💌	Start	🛛 🛛 🥐 🔛 Digital Ser	ial AO Advanced							×				
Device	Ch0: 100m Vrms ~ ^	Audio			Clocks		Bi	t Clock Edge Syne		_				Name CLR
No Device	Ch1: 100m Vrms V	O Single Da	ta Line (TDM)		Master Clk Sou	arce: Internal	~	Outs: F	Rising					
Output Channel Control	Level Track Ch0	01020	304											
Ch1: Ch1: Enable		O Multiple E	Data Lines		Master Clk P	Rate: 49.152M Hz		Ins: I	Rising					
Ch2: Ch2: Enable		Channel	s: 8 🗸 📈 M	ISB First										
Ch3: V Enable				-										
Ch4: 🗹 Enable 🗸	_ Test Set	Forma	it: 12S	~	Al Bit & Frame	Dir: Out	~							
Advanced Setting	Waveform: Sine	Justificatio	n: Left Justified	~										
Stimulus Device	11.15		0.010		Frame Clk R	Rate: 48k Hz								
Output Sample Rate	Frequency: IK nz	Frame puls	e: One Subtrame	× 1										
48 kHz V		Frame Cl	k: 🗸 Invert 🗸 S	hift Left						0.4	0.5 0.6	0.7 0.8	3 0.9 1	$\longleftrightarrow \longrightarrow$
				1000										
		Word Widt	h: 32	*										
Input Configuration			24											Name CLR
Input Configuration		Bit Dept	h: 24	×				Si	ave Cancel					
Connector	FFT Width: 0.2 S	Low N.												
Digital Senal IO	Window: Hanning V	Bitclk		11111										
No Device	Weighting: Linear	Frame												
Input Channie Control	Restart Averaging	Data1	MSE	((Ch: O		LSB						
Ch0: 🗹 Enable 🛆	Advanced													
Ch1: 🗹 Enable	Advanced													
Ch2: 🗹 Enable	Filter Setting													<
Ch3: 🗹 Enable	Recorder:									r	10000		1000	00
Ch4: 🗹 Enable 🗸		4							F					
Advanced Setting														
Sensor Set			Frequency	dBV	dBFS	Rms	dBSPL	dBu	W	SINAD (dB)	THD(%)	THD(dB)	THD+N(%)	THD+N(dB)
		Ch 0									_			
Input Sample Rate		Ch 1												
40 KHZ														
v											Output: Digit	al Serial IO (8 Ch)	24kHz Input: Digit	al Serial IO (8 Ch)2d



Audio

Single Data Line:选择使用的Data数量,可选1或2,此处配置对应为SigmaStudio里节点的的TX/RX引脚 Channel:TDM mode 每组DATA数据传输数量,最大为16 MSB First: 数据第一位为高位 Justification: 选择数据左/右对齐 Frame pulse width: 帧脉冲宽度 Frame invert: 帧反转 Frame shift left::帧左移 Word width:字宽,最高32位 Bit Depth:位深,最高32位

Clocks

Master Clk source:MCLK的时钟方向,可以外部/内部 AO Bit&frame Dir:选择AO的BLCK的时钟方向 AI Bit&frame Dir:选择AO的BLCK的时钟方向(AO和AI输出时,只能选择其中一个OUT) Bit Clock Edge Sync:数据和BCLK的同步方向,可选在BCLK上升沿或者下降沿同步

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